# ServerWorks ServerSet™ III HE
# Product Overview

| Features | Benefits |
|---|---|
| 133 MHz Front Side Bus Capability | • Supports 100 MHz and 133 MHz system bus for single, dual, and quad processor configurations<br>• Significantly increases bandwidth required for multiprocessor servers |
| PC133 SDRAM Technology | • Superior memory performance in terms of bandwidth and access latency<br>• Increases flexibility of system design for memory configurations<br>• Proven technology with low cost structure |
| Server Optimized Memory Technology (Up to 16-GBytes) | • High Bandwidth 4-way interleaved architecture achieves up to 4.1 GBytes/s<br>• Advanced ECC algorithms that maintain system data integrity<br>• Supports a large capacity of memory up to 16-GBytes<br>• Supports wide range of memory DIMMs including 64, 128, 256, 512-MByte, and 1-GByte |
| Enterprise Chipkill Technology | • Maintains system integrity even with a complete DRAM Chip failure |
| Advanced “Inter Module Bus” (IMB) Technology | • Defined Interconnect from North Bridge to remote PCI IO Bridges<br>• Supports 1 GByte/s operation and low latency IO transactions on full duplex, point to point, source synchronous bus |
| Advanced 64-bit PCI Technology | • Two fully independent 64-bit PCI Buses<br>• Maximizes IO bandwidth for the next generation of 64-bit PCI cards<br>• Supports up to 2 full 64-bit/66 MHz PCI busses<br>• Supports up to 5 64-bit/33 MHz PCI busses |
| Advanced IO Caching Technology | • Increases sustainable PCI bus bandwidth by off loading system resources<br>• Reduces Front Side bus snoop traffic for enhanced multiprocessing performance |
| Legacy 32-bit PCI Technology | • Dedicated 32-bit PCI bus for legacy IO and south bridge interconnect |
| Scalable Architecture | • Increases flexibility of system design for processor, memory, and PCI configurations<br>• Strong architectural foundation that enables a smooth transition to the next generation of server technology (i.e. PCI-X, DDR) |
| Full Peer-to-Peer Support | • Allows full peer-to-peer transactions between PCI busses<br>• Increases options for Intelligent IO and Server Management cards |

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| Integrated IOAPIC | • Removes the need for a separate IOAPIC chip<br>• BOM cost savings, additional board real estate, and increased design flexibility |
| ATA66 | • Enhances HDD access for faster reads and writes |
| 4 USB Ports | • Provides the end user with more options to connect peripherals |
| **ServerSet™ III HE Components:** | **Package:** |
| NB6536 North Bridge 2.0HE . | • 644 Tape Ball Grid Array (TBGA) |
| IB6566 South Bridge | • 352 Plastic Ball Grid Array (PBGA) |
| NB6555IO Bridge 2.0 | • 352 Plastic Ball Grid Array (PBGA) |
| NB6535 Memory Address Data Path (MADP) | • 256 Plastic Ball Grid Array (PBGA) |

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